

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FOET 20 09640660

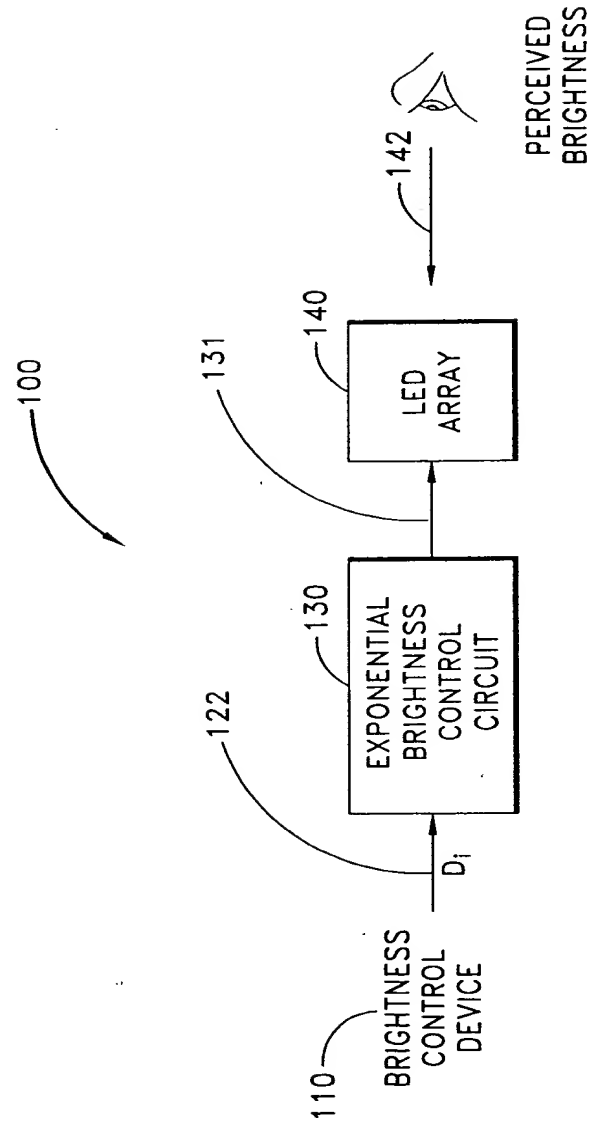


FIG. 1

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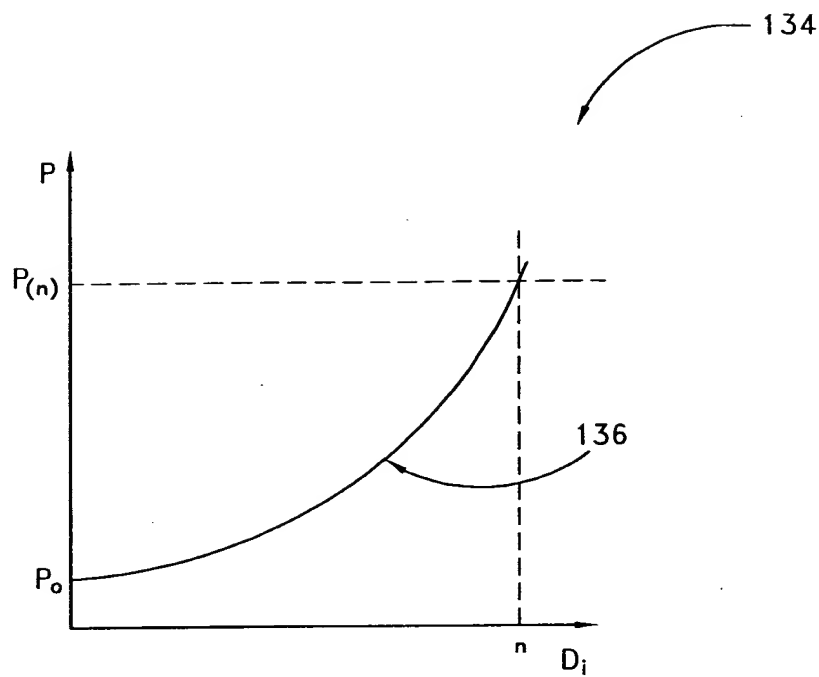


FIG. 2

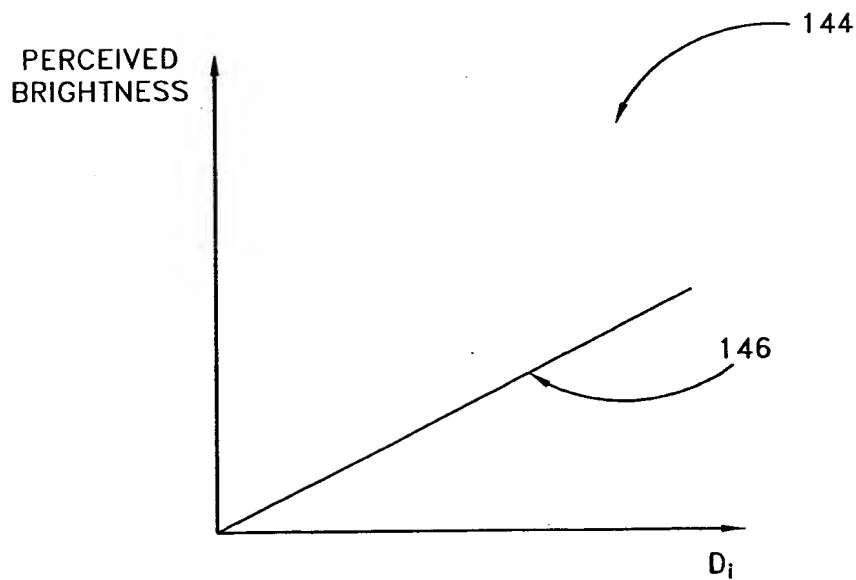


FIG. 3

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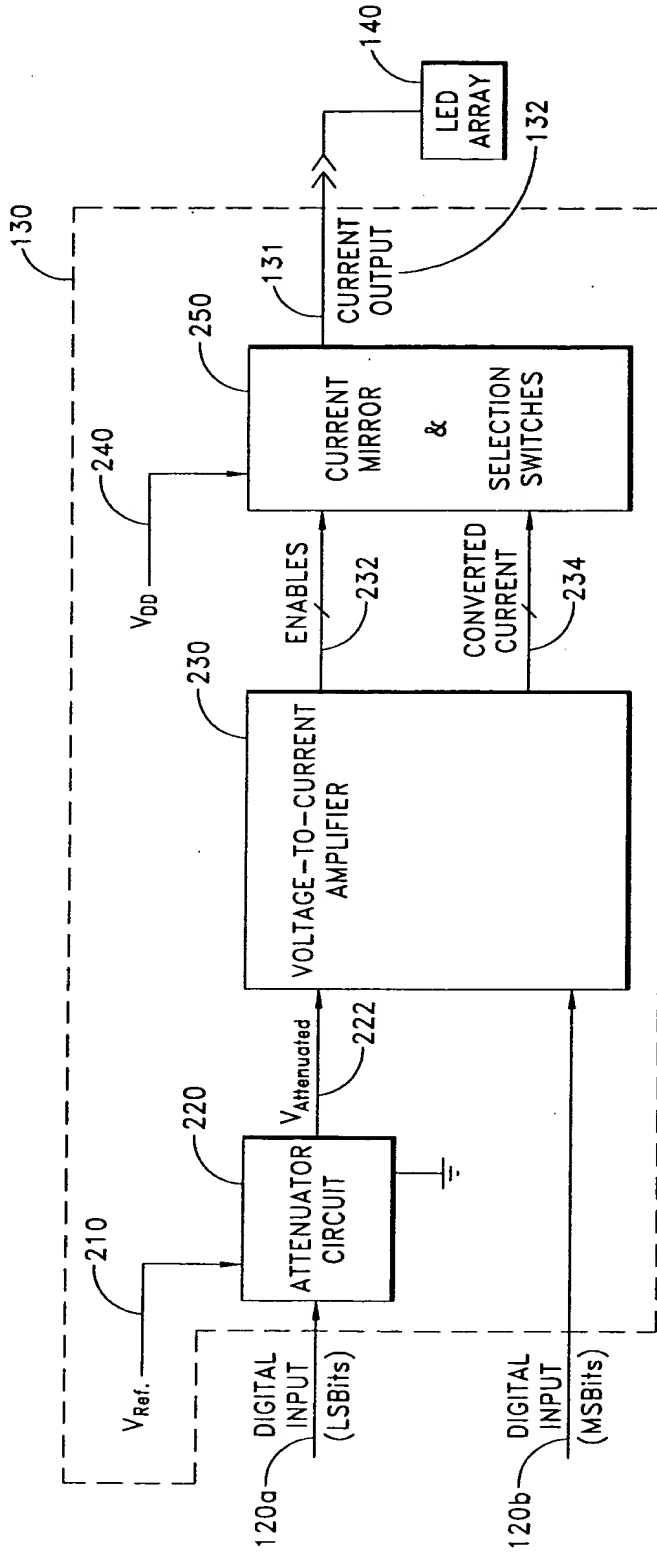


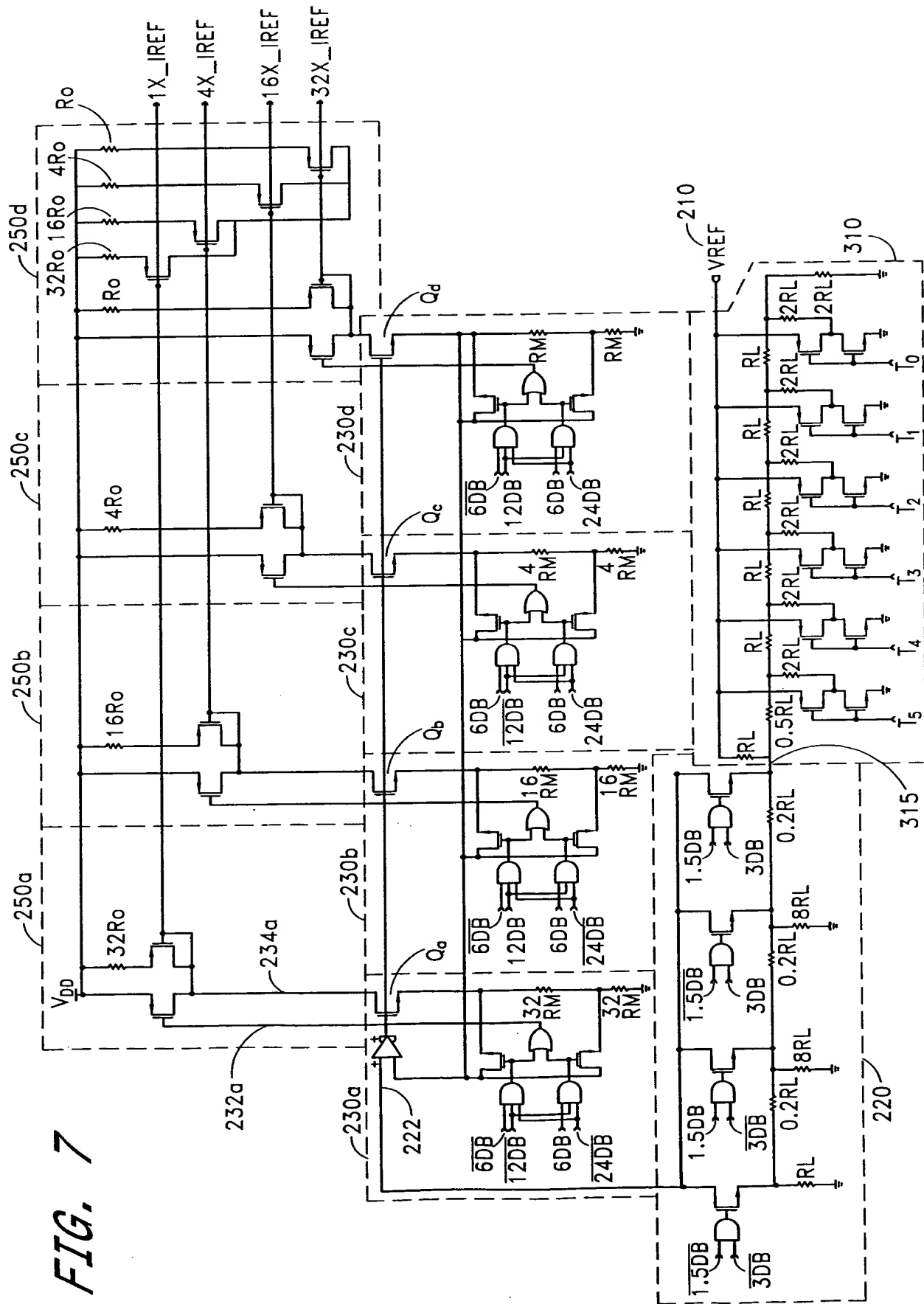
FIG. 4

FOOTNOTES

FIG. 5

The diagram illustrates a 2-bit current source array 200. It includes a reference current source 210 and four current sources 220, 230a, 230b, and 234a. Each current source is implemented with a PMOS transistor (Q_{A1} to Q_{A4}) and a network of NMOS transistors (Q_{VC1} to Q_{VC6}) and resistors (R_A, R_G). The output current of the array is labeled CURRENT_OUTPUT 132. The diagram shows how the current sources are connected to a common output node and how the NMOS transistors and resistors are used to generate the current sources.

FIG. 7



SCANNED, #3

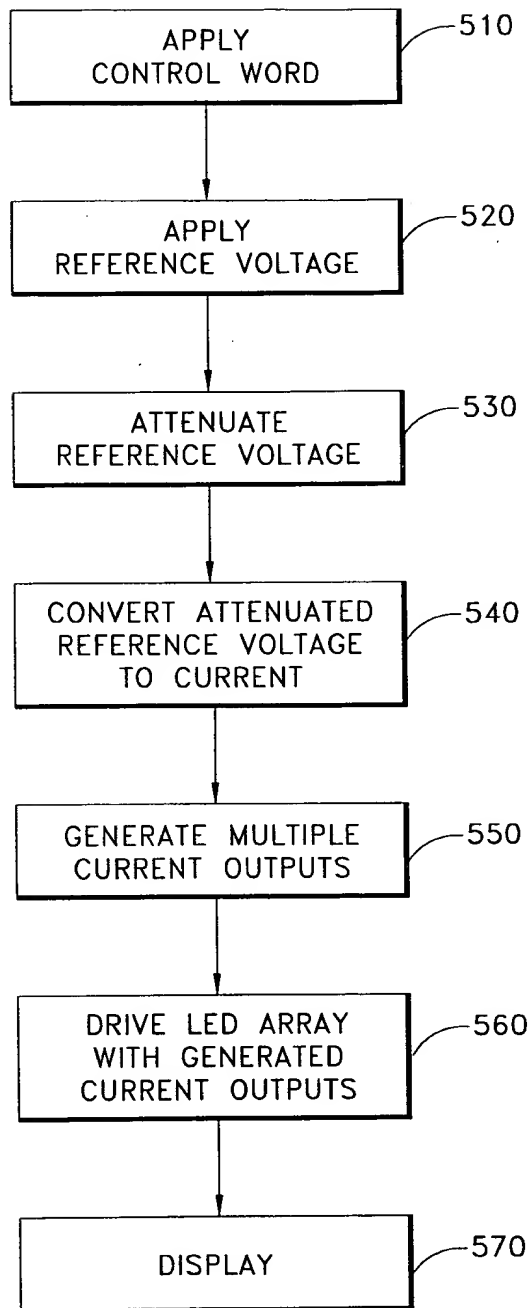


FIG. 8